Code: 9D06106c

M.Tech I Semester Supplementary Examinations February/March 2018

LOW POWER VLSI DESIGN

(Common to DSCE & DECS)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks

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1 (a) What are the various aspects to be considered in low-power design? Explain.
(b) Explain about the design limitations imposed on low power. Low voltage circuits pertaining to the following parameters: (i) Power supply voltage. (ii) Threshold voltage.
(c) What are the advantages of SOI CMOS technology compared to bulk CMOS technology? Explain with necessary graphs.

2 (a) Explain about the isolation requirements in Bi-CMOS process.
(b) Compare double diffused drain and lightly doped drain.

3 (a) Why leakage power is an important issue in deep submicron technology? With schematic diagrams explain about it.
(b) Give the layout of a 2 X 1 vertical NPN BJT, and draw the associated cross-sectional view, with explanation.

4 (a) Explain about the experimental characterization of sub-half micron MOS devices.
(b) Describe the sub threshold current model of MOSFET.

5 (a) Discuss the characterization and power consumption of CMOS gates.
(b) Draw the circuit for high performance complimentary coupled BICMOS circuit for three input NAND logic gate and explain the same.

6 (a) Explain different sources of power dissipation in digital CMOS circuit.
(b) Explain the basic concepts of supply voltage scaling.
(c) Explain the ratio-logic using only nMOS and pseudo nMOS logic network. Compare its advantages and disadvantages with respect to standard static CMOS circuits.

7 (a) Explain about the optimization theme and performance themes of latches.
(b) Give the design perspective for edge triggered D-flip flop.

8 (a) Floating body effects may also cause the parasitic bipolar leakage current in CMOSO-SOI pass gate transistor-Explain.
(b) What are the various ways to reduce the delay time of a CMOS inverter?
(c) How is power consumption is reduced in SRAM to achieve the performance?

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