This question paper contains **4+1** printed pages]

Roll No. | | | | | | | | | | | |

S. No. of Question Paper : **7797**

Unique Paper Code : **2341102** **F-1**

Name of the Paper : **Computer System Architecture (CSDC1-102)**

Name of the Course : **B.Tech. (Computer Science) [DC-1.2]**

Semester : **I**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. **1** is compulsory.

Attempt any *four* questions from question numbers **2** to **7**.

Section A

1. (*a*) Convert $(a \times b) + (c \times d)$ from infix to Reverse Polish Notation (RPN) showing different steps of stack. 4

(*b*) Design and explain the address sequencer for the microprogrammed control unit having control memory of 128 words. There are 4 status bits in the system. Length of microinstruction is 20 bits out of which 9 bits are used for microoperations. 5

(*c*) Formulate a mapping procedure that provides sixteen consecutive microinstructions of each routine of a typical computer. The operation code has five bits and the control memory has 4096 words. 6

P.T.O.

(*d*) The memory unit of computer has 256 K words of 32 bits each. The computer has an instruction format with four fields : an operation code field, a mode field to specify one of the addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instructions in one memory field. 5

(*e*) Explain the following : 4

(*i*) Cycle stealing

(*ii*) Cache mapping

(*iii*) Microoperation

(*iv*) Processor register.

(*f*) Give the differences between isolated I/O and memory-mapped I/O. 3

(*g*) Draw a logic circuit for the following : 2

$$Y = X\bar{Y}Z + XYZ.$$

(*h*) Describe how AND gate can be implemented using NAND gates. 2

(*i*) Explain in detail about associative mapping with the help of example. 4

Section B

2. (*a*) Draw and explain the flow chart of interrupt cycle. Also explain how multiple I/O interrupt is handled in the computer system. 5

(*b*) The control memory has 2048 words of 32 bits each. Each microinstruction has three fields. Three field's microoperations are specified by 15 bits.

(*i*) How many bits are there in the control address register ? 3

(*ii*) How many bits are there in the branch address field and the select field ? 2

3. (*a*) Explain (BSA), ISZ and SPA instructions with their respective microopreation. 6

(*b*) A digital computer has a memory unit with a capacity of 16, 384 words of 40 bits each. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no mode bit present). Two instructions are packed in one memory word and a 40 bit Instruction Register (IR) is available in the fetching and executing an instruction for this computer. 4

4. (*a*) Explain the organization of a microprogrammed control unit with the help of a block diagram. 5

P.T.O.

(*b*) What are the purposes of different kind of addressing modes ? Consider a 16-bit processor in which the following appears in main memory, starting at location 200 :

200	Load to AC	Mode
201	500	
202	Next Instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 400. There is also a base register that contains the value 100. The value of 500 in location 201 may be part of the address calculation. Assume that the location 399 contains the value 999; location 400 contains the value 1000, and so on. Determine the effective address and the operand to be loaded for the following address modes :

(*i*) Direct

(*ii*) Immediate

(*iii*) Indirect

(*iv*) PC relative

(*v*) Register. 5

(a) Differentiate between an encoder and a decoder. Construct a 3 × 8 decoder with 2 × 4 decoders. 5

(b) Give the truth table of full adders. Derive the Boolean function of a full adder using Karnaugh Map. Hence draw its circuit diagram. 5

5. (a) Differentiate among Main memory, Control memory and Cache memory. 3

(b) Give the differences between hardwired control and microprogrammed control processors architectures. 3

(c) Give I/O channel architecture with the help of diagram. 4

6. (a) Give block diagram of DMA controller. How does CPU initialize the DMA transfer ? 6

(b) A two-way set associative Cache memory uses blocks of four words. The Cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K*32. What are the sizes of the : 4

(i) TAG

(ii) INDEX ?