Code: 9D06106c

M.Tech II Semester Supplementary Examinations February 2018

LOW POWER VLSI DESIGN

(Electronics & Communication Engineering)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) What you mean by low power design? Explain why it is so important.
(b) Justify the statement 'SOI is one of the leading technology'.

2 Describe the following MOS transistor isolation techniques:
(a) LOCOS.
(b) Shallow trench isolation
(c) Deep trench isolation.

3 With the help of cross-sectional diagram, illustrate the features of modern CMOS technology.

4 Explain in detail the EKV MOSFET and advanced MOSFET model.

5 Implement a 3-input NAND gate using the following logics:
(a) CC-BiCMOS.
(b) FS-BiCMOS.
(c) FS-CMBL.

6 (a) Perform comparative analysis of all the BiCMOS circuit in terms of power, delay and voltage swing.
(b) Draw and explain a charge-pump integrated Hβ-BiCMOS circuit.

7 Implement the clocked SR flip flop in the following styles:
(a) A fully static.
(b) A RAM style.
(c) A CVSL style.

8 Describe the following with respect to power reduction in clock networks:
(a) Clock gating.
(b) Reduced swing clock.
(c) Oscillator circuit for clock generation.

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