Code: 9D06203

M.Tech II Semester Supplementary Examinations February 2018

DESIGN OF FAULT TOLERANT SYSTEMS

(Digital Systems and Computer Electronics)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Derive relation between reliability and MTBF.
(b) Derive reliability of the following systems:
(i) Series. (ii) Parallel. (iii) Parallel-series. (iv) Series-parallel.

2 (a) Discuss about static and dynamic redundancy techniques with neat diagrams.
(b) Discuss about self purging redundancy technique.

3 (a) Design a totally self checking checker.
(b) Design a self checker circuit using m out of n codes.

4 Give the design procedure for a totally self checking PLA.

5 (a) Define the terms: (i) Testability. (ii) Observability.
(b) Discuss about Reed Muller's expansion technique with an example.

6 With a neat diagram, discuss about a signature analyzer using an LFSR.

7 With a neat diagram, discuss about level sensitive scan design (LSSD).

8 Write short notes on the following:
(a) Exhaustive testing.
(b) Pseudorandom testing.

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