Code: 9D06206c

M.Tech II Semester Supplementary Examinations February 2018

FPGA ARCHITECTURE & APPLICATIONS

(Digital Systems and Computer Electronics)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Implement the following Boolean function using PAL:

$$F(w,x,y,z) = \sum_m (0,2,4,6,8,10,11,12,14,15)$$

(b) Distinguish between FPGA and CPLD.

2 (a) Explain a Govt. state assignments for FPGA.

(b) Realize switching functions (2, 3, 4, 6, 7) using 2 input LUTS. Give the truth table implementation in each LUT & show wires in FPGA.

3 (a) Write about FPGA and compare speed performance of ACT1, ACT2, ACT3 FPGA.

(b) What is LE? Draw and explain the working of LE of altera FLEX 8000.

4 (a) What is state transition table?

(b) Explain how state transaction assignment can be carried at for FPGA.

5 (a) Explain the procedure for design of a state machine using one-hot encoding.

(b) Explain the symbolic representation of FSM architectures.

6 Write notes on:

(a) Architecture centred around non registered PLDs.

(b) State machine design centered around shift registers.

7 (a) Design a parallel adder sequential circuit.

(b) Explain multiplexers.

8 Write notes on:

(a) Counters and parallel controllers.

(b) Combinational logic circuits.

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