Code: 9D06106c

M.Tech II Semester Supplementary Examinations January/February 2017

LOW POWER VLSI DESIGN

(Electronics & Communications Engineering)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain different sources of power dissipation in digital CMOS circuit.
(b) Explain sub threshold swing.

2 (a) With neat diagram, explain n-well and channel formation in CMOS process.
(b) What are the technology and device innovations available to reduce total capacitance?

3 (a) Discuss the transistor sizing and gate oxide thickness.
(b) List out second order effects of MOS transistor.

4 Write a note on the following terms:
(a) Static state power.
(b) Gate level capacitance estimation.

5 (a) Give a brief note on CMOS fabrication steps with necessary diagram.
(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expression.

6 (a) Compare CMOS dynamic domino and pseudo nMOS logic families.
(b) Write short notes on pulsed latches and its timing metrics.

7 (a) Design a D-latch using transmission gate.
(b) Develop the necessary stick diagram and layout for the design of inverter, NAND and NOR gates.

8 (a) Explain different precharge techniques employed by SRAM.
(b) A 32 bit off-chip bus operating at 5v and 66 MHz clock rate, is driving capacitance of 25 picoF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus?

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