Code: 9D06203

M.Tech II Semester Supplementary Examinations January/February 2017

DESIGN OF FAULT TOLERANT SYSTEMS

(Digital Systems and Computer Electronics)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks

*****

1 (a) Derive the relationship between reliability and mean time between failures (MTBF).
(b) Derive the expression for reliability of a parallel combinational circuit.

2 (a) Discuss about static and dynamic redundant systems with necessary diagrams.
(b) With a neat diagram, discuss about Sift-out redundancy technique.

3 Design a self checking checker using Berger code with an example.

4 Design a sequential circuit for fail-safe design using partition theory.

5 Discuss the design of a combinational circuit for testability using control and syndrome testable design.

6 Discuss about an LFSR based signature analyzer with a neat diagram.

7 Explain how controllability and observability are obtained by means of scan register with an example.

8 Discuss about test pattern generation for BIST exhaustive testing with an example.

*****