Code: 9D06101

M.Tech I Semester Regular & Supplementary Examinations February 2016

DIGITAL SYSTEM DESIGN

(Common to DSCE, DECS, ECE, VLSIES, ESVLSI, VLSIESD & MNE)

(For students admitted in 2011, 2012, 2013, 2014 & 2015 only)

Time: 3 hours Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Discuss the primary constructs that are used in VHDL.

(b) Design a 4 X 3 ROM to perform:

$F_1 = \sum(0, 1, 2, 3, 7)$

$F_2 = \sum(1, 2, 3, 5, 7)$

$F_3 = \sum(0, 2, 4, 6)$

2 (a) Draw the symbols used in ASM chart and explain.

(b) Describe important features of FPGA.

3 Construct the test set of output function of the circuit $F(X_1, X_2, X_3) = X_1X_3 + (\overline{X_2 + X_3})$. Using path sensitizing method.

4 (a) With a neat circuit diagram, describe the working of a signature analyzer.

(b) Write short notes on testing for bridging faults.

5 (a) Explain about fault detection and location in sequential circuits.

(b) Discuss about synchronizing experiments of fault diagnosis in sequential circuits.

6 (a) Explain the various types of cross point fault that occur in PLA's.

(b) Explain PLA folding.

7 (a) Explain how test generation can be achieved in testing a PLA.

(b) Discuss briefly about testable PLA design.

8 Explain the fundamental mode model for asynchronous sequential machine design.

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