Code: 9D06206b

M.Tech II Semester Supplementary Examinations January/February 2017

ALGORITHMS FOR VLSI DESIGN AUTOMATION

(Digital Systems & Computer Electronics)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks

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1 (a) List and explain any two design automation tools.
(b) How graph theory is useful for VLSI design automation.

2 (a) Why combinational optimization is required? Explain the principle of backtracking.
(b) How combinatorial optimization is achieved using local & Tabu search.

3 (a) Explain the concept of layout compaction bringing out clearly, how compaction is useful for VLSI design.
(b) Explain the routing problems in floor planning methods of VLSI design.

4 (a) Explain how gate level modeling is inferior/superior to switch level modeling.
(b) Write about the compiler-driven simulation.

5 (a) Explain the basic issues and terminology involved in logic synthesis and verification.
(b) Explain two-level logic synthesis with suitable examples.

6 (a) How allocation, assignment and scheduling are done in high level synthesis?
(b) Explain high level transformations related to high level synthesis.

7 (a) Explain the physical design cycle of FPGA.
(b) Explain about partitioning for segmented models.

8 Explain briefly:
(a) MCM physical design cycle.
(b) Maze routing.
(c) Programmable MCM.

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