Code: 9D06206c

M.Tech II Semester Supplementary Examinations January/February 2017

FPGA ARCHITECTURE & APPLICATIONS

(Digital Systems & Computer Electronics)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain about FLEX logic with the aid of suitable sketch.
(b) Explain in detail about mask programmable ROM.

2 (a) Write notes on technology mapping for FPGAs with suitable example.
(b) Explain routing architecture of FPGA.

3 (a) Explain the design considerations of Xilinx XC4000 series FPGAs with relevant example.
(b) Draw and explain the operation of Xilinx based XC 4000 CLB.

4 (a) With suitable example, explain the top down design approach for FPGAs using finite state machines.
(b) Elaborate the derivations of state machine charts relevant to FSM with suitable example.

5 (a) Discuss about meta stability and synchronization of finite state machines.
(b) Write an example and explain about one-hot design using ASM.

6 Draw and explain the model used for architecture centered around nonregistered programmable logic devices.

7 (a) Explain the concepts of controller, data path and functional partition with respect to system level design.
(b) Give the design flow of FPGA as a case study of counter.

8 Give the design flow of FPGA as a case study of parallel adder and parallel controller.

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