

Code: 17D06109

M.Tech II Semester Supplementary Examinations January/February 2019

**TEST & TESTABILITY**

(Common to VLSI, VLSIS &amp; VLSISD)

(For students admitted in 2017 only)

Time: 3 hours

Max. Marks: 60

Answer all the questions

\*\*\*\*\*

- 1 (a) Classify types of testing and explain in brief about them.  
(b) Explain in brief about bridging faults.

**OR**

- 2 (a) Explain about the types of testing of VLSI chips.  
(b) Explain in detail about temporary faults.

- 3 (a) Illustrate serial fault simulation for large number of faults.  
(b) Illustrate detective fault simulation using combinational circuit.

**OR**

- 4 (a) Explain about event driven simulation using combinational circuit.  
(b) Illustrate two valued deductive simulation with example.

- 5 (a) Explain concept of controllability and observability with the help of block diagram.  
(b) Compute the combinational SCOAP testability measures for the circuit that realizes an expression  $J = ((A+B) \oplus E) + BC + D$ .

**OR**

- 6 (a) Illustrate partial-scan design with s-graph.  
(b) Explain about the properties of Ad-Hoc DFT method and its difficulties too.

- 7 (a) Illustrate economic case for BIST.  
(b) Explain about the process of random pattern generation.

**OR**

- 8 (a) Illustrate circular self-test path BIST architecture with example.  
(b) Illustrate LFSR as signature analyzer.

- 9 (a) Explain boundary register cell with neat schematic.  
(b) Explain BYPASS and INTEST instructions in boundary scan description language.

**OR**

- 10 (a) Explain about BDSL description components.  
(b) Explain about ring configuration of TAP controller.

\*\*\*\*\*