

Code: 17D06201

M.Tech II Semester Supplementary Examinations January/February 2019

EMBEDDED SYSTEM DESIGN

(Common to DECS, ECE, DSCE, VLSI, VLSIS & VLSISD)

(For students admitted in 2017 only)

Time: 3 hours

Max. Marks: 60

Answer all the questions

- 1 What is embedded system? Explain embedded system design and development life cycle.
OR
- 2 Explain ISA architecture models, processor design and memories of embedded processors.
- 3 With neat sketches, explain the architecture of MSP430 processor.
OR
- 4 Explain the addressing modes and instruction set of MSP430 processor.
- 5 Explain the interfacing mechanism of MSP430 processor with digital inputs and outputs.
OR
- 6 What is watchdog timer? Explain Timer-A and Timer-B modes of operation.
- 7 Explain the interfacing mechanism of SPI with USCI.
OR
- 8 Explain inter integrated circuit bus and its operation.
- 9 What is UART? Why we use UART? And explain UART architecture.
OR
- 10 Explain analog to digital interfacing mechanism in MSP430.
