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M.Tech II Semester Supplementary Examinations January/February 2019 CPLD & FPGA ARCHITECTURES & APPLICATIONS

> (Digital Systems & Computer Electronics) (For students admitted in 2017 only)

Time: 3 hours

Max. Marks: 60

Answer all the questions

- 1 (a) Explain the various architectures of Xilinx Cool Runner CPLDs.
 - (b) Distinguish between programmable logic devices.

OR

- 2 (a) Write short notes on CPLD implementation of a parallel adder with accumulation.
 - (b) Realize 3 X 8 decoder with single enable input using PAL & PLA.
- 3 (a) With neat diagrams, explain logic block architectures of FPGAs.
 - (b) Write a short note on applications of FPGAs.

OR

- 4 (a) Explain the concept of programmable I/O blocks in FPGAs.
 - (b) Explain different programming technologies in FPGAs.
- 5 (a) Write about SRAM programming technology of programmable FPGAs with neat sketches.
 - (b) List out the salient features of Xilinx based XC 3000 CLB.

OR

- 6 Draw the schematic diagram of Xilinx based XC 4000 CLB and describe its functional operation.
- 7 (a) Discuss the architectural differences of ACT1 and ACT2 family FPGAs.
 - (b) Explain how anti-fuse programming technology is used in Actel FPGAs.

OR OR

- 8 (a) How would you implement a binary counter using the CLBs of FPGA?
 - (b) Describe the applications of Actel FPGAs.
- 9 (a) Explain about position tracker of a Robot manipulator with help of FPGAs.
 - (b) Realize full adder using Actel FPGAs.

OR

10 Explain about a fast video controller.
