Code: 17D06207

M.Tech II Semester Supplementary Examinations January/February 2019

SYSTEM ON CHIP DESIGN

(Digital Systems and Computer Electronics)

(For students admitted in 2017 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1	(a)	Mention the instruction execution sequence of processor.	
	(b)	List out the SOC memory considerations.	
		OR	
2		Comprehend the pipelined processor model.	
3		Draw and explain the block diagram of processors in SOC model.	
		OR	
4		List out the instruction set mnemonic operations.	
5	(a)	Write about the WRITE policies of memory design.	
	(b)	Write about basic DRAM types.	
		OR	
6		Write about simple DRAM and their memory array.	
7		Draw the simplified block diagram of an SOC module and explain.	
		OR	
8	(a)	Compare the bus interconnect architectures.	
	(b)	Write about commercial logic block architecture of Xilinx CLB.	
9		Draw and explain the block diagram of JPEG compression.	
		OR	
10		Write about performance and Area trade-off on Xilinx vertex XCV-1000	

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