**Code: 17D06210**

M.Tech II Semester Supplementary Examinations January/February 2019

**LOW POWER VLSI DESIGN**

(Digital Systems & Computer Electronics)

(For students admitted in 2017 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 Explain the need for low power VLSI design.

**OR**

2 What are the sources of power dissipation in digital IC's? Explain.

3 Discuss about pipelining and parallel processing approaches.

**OR**

4 What is the difference between MTCMOS and VTCMOS? How it will effect in the reduction of power in designing multiplexer and flip-flops?

5 Describe about CMOS adder's architecture.

**OR**

6 Explain about low voltage low-power design techniques.

7 Draw the basic building blocks of the Baugh-Wooley multiplier architecture and explain its operation.

**OR**

8 Explain about Booth multiplier.

9 Discuss sources of power dissipation in SRAM and DRAM.

**OR**

10 With neat diagrams, explain about SRAM technologies and DRAM architecture.

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