Code: 9D06106c

M.Tech II Semester Supplementary Examinations August/September 2018
LOW POWER VLSI DESIGN
(Electronics & Communication Engineering)
(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours   Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks
*****

1   Explain the limitations of low-voltage, low-power design w.r.t the following:
(a)   Power supply voltage.
(b)   Threshold voltage.
(c)   Scaling.
(d)   Interconnect wires.

2   (a)   What are the considerations to be taken care while integrating BiCMOS process? Explain.
    (b)   Discuss briefly the p-well CMOS process and Twin-well Bi-CMOS process.

3   Illustrate a $0.2~\mu m$ SOI BiCMOS process flow and then explain each step of it.

4   Explain in detail the current model of advanced MOSFET model.

5   Discuss the following basic driver configurations of BiCMOS logic circuit:
(a)   The common-emitter.
(b)   The gated diode.
(c)   The emitter follower.

6   (a)   Design ESD-free BiCMOS inverter and then explain the same.
    (b)   Compare performance of ESD-free BiCMOS digital circuit with an optimized two-stage CMOS and the TS-FS-BiCMOS circuits.

7   (a)   Explain the pipelining theme by taking a negative edge-triggered C^2MOS flip-flop.
    (b)   Develop a dynamic negative-edge triggered flip-flop based on pass transistor logic and then explain the same.

8   Describe the following low power techniques for SRAM:
(a)   Memory bank partitioning.
(b)   Pulsed word line and reduce bitline swing.

*****