



M.Tech II Semester Supplementary Examinations August/September 2018

DESIGN OF FAULT TOLERANT SYSTEMS

(Digital Systems & Computer Electronics)

(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks

- 1 Write a short note on following:
 - (a) Reliability.
 - (b) Meantime.
 - (c) Maintainability.
 - (d) Availability.
- 2
 - (a) Discuss about triple modular redundancy with necessary diagrams.
 - (b) Explain time redundancy and sift out redundancy.
- 3
 - (a) What is self-checking circuits? Explain the principle of operation of a self-checking circuit with a suitable diagram.
 - (b) Design a totally self-checking checker using low cost residue code.
- 4
 - (a) Explain fail safe design of sequential circuits using Berger code.
 - (b) Explain the fail-safe design of synchronous sequential circuits using partition theory.
- 5
 - (a) Design the circuit for the Reed-Muller expansion implementation.
 - (b) Explain use of control and syndrome testable design for combinational circuits.
- 6 Discuss about theory and operation of linear feedback shift register with a suitable diagram.
- 7
 - (a) Explain controllability and observability with scan register with a suitable diagram.
 - (b) Explain classic scan design.
- 8
 - (a) Discuss test pattern generation for BIST with examples.
 - (b) Explain constant weight patterns.
