Code: 9D06206b

M.Tech II Semester Supplementary Examinations August/September 2018
ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Digital Systems and Computer Electronics)
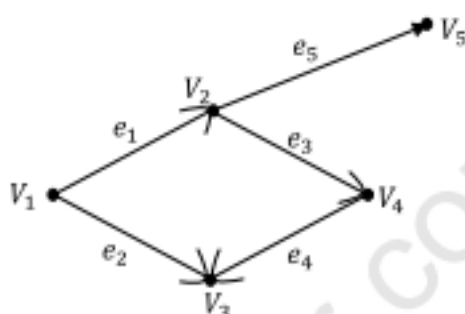(For students admitted in 2013, 2014, 2015 & 2016 only)

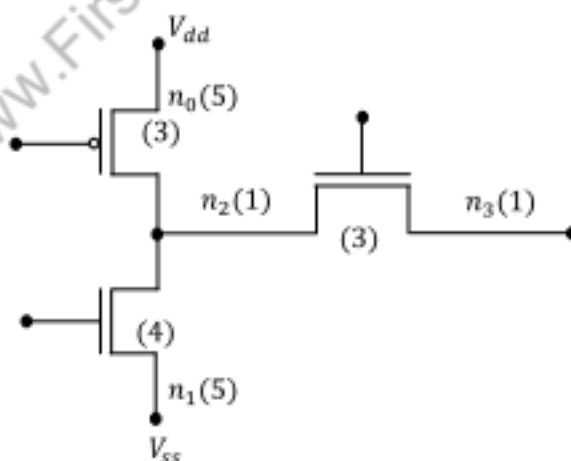Time: 3 hours   Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks
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1 (a) For the graph shown below, determine the edges using depth – first search algorithm.
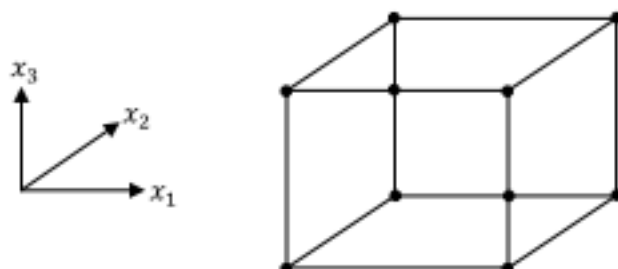

   (b) Write the pseudo code for the breadth – first search algorithm.

2   Differentiate between backtracking and branch & bound algorithm. Also write the pseudo code for both.

3 (a) Write the pseudo code for longest path algorithm.
   (b) Explain, how graph – theoretical formulation is framed.

4 (a) Write a pseudo code of the event – driven simulation function.
   (b) Illustrate the switch level simulation algorithm for the following circuit.

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5   Write truth table function for the following set Boolean function f in B^3 and also evaluate step by step using ROBDD – Building algorithm.

6   Explain in detail force – directed scheduling.

7   With neat diagram, explain physical design cycle of FPGA.

8   Explain multiple stage routing.

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