Code: 9D06206c

M.Tech II Semester Supplementary Examinations August/September 2018

FPGA ARCHITECTURE & APPLICATIONS

(Digital Systems and Computer Electronics)

(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Write about Altera series – max 5000 / 7000 series CPLD'S in detail.
(b) Explain speed performance and in system programmability of lattice PLSI'S architecture.

2 (a) Explain the mapping technology for FPGA.
(b) What is an FPGA? Give the advantages and applications of FPGA.

3 (a) Discuss the design aspects of Altera flex FPGA 8000.
(b) Compare different versions of ACT – 1, 2, 3.

4 (a) What is a state assignment problem? Explain with example.
(b) Explain about top down design flow of FSM.

5 (a) Explain the basic concepts and properties of petrinet for state machine.
(b) Define meta stability.

6 (a) Explain the use of ASMs in one hot design.
(b) Describe the state machine design approach centered around shift registers.

7 Show the design flow using FPGA as a case study for: (i) Counters. (ii) Multiplexers.

8 List out the salient features of mentor graphics EDA tool "FPGA ADVANTAGE".

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