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Code: 9D06106c

M.Tech I Semester Regular & Supplementary Examinations February 2016

LOW POWER VLSI DESIGN

(Common to DSCE & DECS)

(For students admitted in 2011, 2012, 2013, 2014 & 2015 only)

Time: 3 hours Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) What are the factors that make power as an important design constraint in today's VLSI design? List and explain.

(b) What are the advantages and disadvantages of Silicon-on-insulator?

2 (a) Draw the cross sectional diagram of optimized twin-well BiCMOS structure and explain the process.

(b) Describe integrated digital CMOS process.

3 (a) What are the advantages of copper inter connects for deep submicron CMOS/BiCMOS structures.

(b) Explain about low power CMOS circuit design technique.

4 (a) Discuss about MOSFET model parameters related to trans-conductance.

(b) What are the limitations of MOSFET models? Mention some of MOSFET model applications.

5 (a) Draw the circuit diagram of common emitter BiCMOS drive configuration and explain the operation with $I_{SD} - V_{SD}$ characteristics.

(b) Draw the circuit diagram of two-input CMOS NOR gate and explain its operation with the help of truth table.

6 (a) Compare the advanced BiCMOS NAND (two input) implementations with neat circuit diagram.

(b) Briefly explain about ESD – free BiCMOS circuits.

7 (a) Explain about design quality measures for latches and flip flops.

(b) Draw a transmission gate based dynamic flip flop and explain its operation.

8 (a) Discuss about power reduction process in clock networks.

(b) Describe the power consumption in a 4-transistor SRAM cell.

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