B.Tech III Year I Semester (R13) Supplementary Examinations June 2016

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Classify the logic family by operation.
(b) Which is the fastest logic gate? And why?
(c) What is the necessity of simulation? Mention different types of simulation.
(d) Explain primary constructs in VHDL?
(e) List the applications of multiplexers and demultiplexers.
(f) Why totem pole outputs cannot be connected together?
(g) What is race around condition?
(h) Define setup time and hold time.
(i) Define PLD. Give its classification.
(j) Define ROM and programmable logic array. Differentiate them.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation.
(b) Explain how a CMOS device is destroyed.

OR

3 (a) Discuss about CMOS dynamic electrical behavior with characteristics.
(b) Mention the DC noise margin levels of ECL 10K family.

UNIT – II

4 (a) Explain the difference in program structure of VHDL and any other procedural language. Give an example.
(b) Explain the behavioural design model of VHDL.

OR

5 (a) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.
(b) What is the importance of time dimension in VHDL? Explain its function.

UNIT – III

6 (a) Design a 10 to 4 encoder with inputs 1- out of 10 and outputs in BCD. Provide the data flow style VHDL program.
(b) Explain about combinational multipliers.

OR

7 (a) Design a full subtractor with logic gates and write VHDL data flow program for the implementation of the above subtractor.
(b) Describe three state devices.

UNIT – IV

8 (a) Describe dual parity encoder.
(b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop? Write data-flow style VHDL program.

OR

9 (a) Design an 8-bit serial-in and parallel-out shift register with flip-flops. Explain the operation with the help of timing waveforms.
(b) Write VHDL data-flow program for the above shift-register.

UNIT – V

10 (a) Explain the internal structure of 64Kx1 DRAM. With the help of timing waveforms discuss DRAM access.
(b) Explain the functional behavior of Static RAM cell.

OR

11 (a) With the help of timing waveforms, explain read and write operations of static SRAM.
(b) Discuss how PROM, EPROM and EEPROM technologies differ.

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