Code: 13A05401 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations June 2016

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Differentiate high level language, assembly language and machine language.
(b) What is the role of operating system?
(c) List the different addressing modes used in a basic computer.
(d) What is an overflow in arithmetic operation of signed magnitude data? How is it detected?
(e) What is register transfer language?
(f) Write the microinstruction format.
(g) Define hit ratio.
(h) What is a strobe signal?
(i) Define parallel processing and pipelining.
(j) Differentiate between Multiprocessors and Multicomputers.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain about memory subsystem organization.

OR

3 Explain about I/O subsystem and interfacing.

UNIT – II

4 Discuss in detail about the memory reference instructions of a basic computer.

OR

5 Show the step-by-step multiplication process using Booth algorithm when (-9) and (-13) are multiplied. Assume 5 bit registers to hold signed numbers and (-9) to be the multiplicand.

UNIT – III

6 Design a digital circuit that performs the four logic operations of AND, OR, Exclusive –OR and NOT. Show the logic diagram of one typical stage.

OR

7 Explain in detail about the organization of microprogram sequencer and how it is used for address sequencing in a microprogrammed control unit.

UNIT – IV

8 What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory.

OR

9 What is DMA? Explain the DMA transfer using neat diagram.

UNIT – V

10 Explain briefly about arithmetic pipeline with neat diagram.

OR

11 Discuss in detail about the multiport memory interconnection structure used in multiprocessors.

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