Code: 9A04401 **R09**

B.Tech II Year II Semester (R09) Supplementary Examinations May/June 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Explain the 7 bit Hamming code.
(b) A receiver with even parity Hamming code is received the data as 1101101. Determine the correct code.

2 (a) State and prove DeMorgan's laws. Mention gate equivalents.
(b) Determine the sum of minterms canonical form of the following function:
F(A,B,C) = (A' + B)(B' + C)
(c) Implement the Boolean function F = A (B + CD) + BC' using only NOR gates.

3 (a) What are the advantages of Tabulation method over K-map?
(b) Simplify the following Boolean function using Tabulation method.
Y(A,B,C,D) = ∑(0,1,2,3,5,7,8,9,11,14)

4 (a) What is Encoder? Design Octal to Binary Encoder.
(b) Design 5*32 decoder using two 4*16 decoders with block diagram.

5 (a) What are the steps involved to synthesize the Boolean expression?
(b) Write short notes on multi-gate synthesis.

6 (a) What is race-around problem in JK flip-flop? Explain how it is eliminated in Master-Slave J-K flip-flop.
(b) Draw the truth tables and symbols of S-R, J-K, T and D flip-flop.

7 (a) Explain the capabilities and limitations of finite state machines.
(b) Determine minimal state equivalent of state table given below.

PS	NS,Z	
	X=0	X=1
1	1,0	1,0
2	1,1	6,1
3	4,0	5,0
4	1,1	7,0
5	2,0	3,0
6	4,0	5,0
7	2,0	3,0

8 (a) Explain in detail the block diagram of ASM chart.
(b) Draw the portion of an ASM chart that specifies the conditional operation to increment register R during state T1 and transfer to state T2, if control inputs z and y are = 1 and 0 respectively.

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