Code: 9A10504 **R09**

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2016

LINEAR & DIGITAL IC APPLICATIONS

(Common to EEE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Why frequency compensation is required for an op amp and explain frequency compensation technique using suitable diagrams?

(b) Define the terms PSRR, CMRR, slew rate, input bias current, input off set voltage and gain bandwidth product.

2 (a) Write the important features of instrumentation amplifier. Draw a system whose gain is controlled by an adjustable resistance and explain each block.

(b) Explain and draw the output waveforms of the ideal integrator circuit when the input is sine, step and square wave input.

3 (a) Draw and explain the block diagram of PLL. Derive the expression for capture range.

(b) Design a monostable multi vibrator using 555 timer to produce a pulse width of 100 m sec.

4 (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate.

(b) Design a CMOS 4-input OR gate. Draw the logic diagram and function table.

5 (a) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.

(b) Explain the following items with reference to TTL gate:
(i) Voltage levels for logic '1' & logic '0'.
(ii) DC noise margin.
(iii) Low state unit load.
(iv) High state fan out.

6 (a) Explain with an example, the syntax and the function of the following VHDL statements:
(i) Case statement.
(ii) Loop statements.

(b) Explain the use of packages. Give the syntax and structure of a package in VHDL.

7 (a) With the help of logic diagram explain 74 x 157 multiplexer. Write the dataflow style VHDL program for the IC.

(b) Design a two digit BCD adder using logic gates.

8 (a) Explain right shift register using D flip flop with the help of block diagram.

(b) Design a modulo-12 ripple counter using 74 x 74. Write a VHDL program for this logic using data flow style.

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