

B.Tech I Year(R07) Supplementary Examinations, May 2010
BASIC ELECTRICAL AND ELECTRONICS ENGINEERING
(Bio-Technology)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
 All Questions carry equal marks

1. (a) Define the terms
 - i. active power
 - ii. reactive power and
 - iii. apparent power, and give the expressions for the same.
- (b) A single phase motor operating at 440 V, 50 HZ supply is developing 10 kW with an efficiency of 84% and power factor 0.7 lag. Calculate (a) the input KVA and active power, and reactive power. [6+10]
2. (a) Explain the process of voltage build up in a self-excited D.C machine.
- (b) List out the various conditions to be satisfied for voltage build up process in a self-excited machine, and write down remedies if the conditions fail. [8+8]
3. (a) Draw the energy band diagram of p-n junction under open circuit condition and explain its operation.
- (b) Prove that the dynamic resistance of p-n diode is $r \approx \frac{nVT}{I}$ [10+6]
4. (a) Draw the circuit diagram of half wave rectifier and explain its operation.
- (b) A half wave rectifier is fed by 220 V, 50 Hz via a step down transformer of turns ratio 11:1 find
 - i. the output DC and
 - ii. peak inverse voltage under no load condition. [8+8]
5. (a) Compare the merits and drawbacks of FET and BJT.
- (b) Sketch the basic structure of an n-channel JFET.
- (c) Define the pinch off voltage V_P and sketch the depletion region before and after pinch-off and explain the reason. [6+4+6]
6. (a) Compare the differences between voltage amplifiers and power amplifiers.
- (b) Show that the maximum theoretical efficiency of class B push-pull amplifiers is 78.5%.
- (c) Draw the circuit of a transformer coupled power amplifier and explain its operations with help of load-line analysis. [4+6+6]
7. (a) List out the characteristics of OP-AMP.
- (b) Explain about the concept of 'Virtual Ground' in OP-AMPs.
- (c) Draw the circuit diagram of emitter coupled differential amplifier and obtain its DC analysis.. [6+4+6]
8. (a) Explain with a block diagram the major blocks of a digital computer.
- (b) Implement the following with either NAND or NOR gates. Use only 4 gates only the normal inputs are available.
 $F = w'xz + w'yz + x'yz' + wxy'z$.
- (c) With a circuit diagram, explain Counter type A to D converter. [4+6+6]
