Code No: R5210204 **R5**

II B.Tech I Semester(R05) Supplementary Examinations, May/June 2010
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. Convert the following to Decimal and then to Binary.
   (a) 1011_{16}
   (b) $ABCD_{16}$
   (c) 7234_8
   (d) 7766_8
   (e) 128_{10}
   (f) 720_{10}. [3+3+3+3+2+2]

2. (a) Reduce the following Boolean expressions. [8]
      i. ((AB)'+A'+AB)'
      ii. AB+(AC)'+AB'+C(AB+C)
      iii. ((AB'+ABC)'+ A(B+AB'))'
      iv. AB+A(B+C)+B(B+C)
   (b) Obtain the Dual of the following Boolean expressions. [8]
      i. x'y'+xy+x'y
      ii. xy'+y'z'+x'z'
      iii. x'+xy+xz'+xy'z'
      iv. (x+y)(x+y')

3. (a) Simplify the Boolean function using K-map
   F= $\sum m(0, 1, 2, 4, 7, 8, 12, 14, 15, 16, 17, 18, 20, 24, 28, 30, 31)$ [10]
   (b) Simplify the Boolean expression using K-map
   F= $(\bar{A}) + (AB) + (AB\bar{D}) + (A\bar{B}\bar{D}) + (C)$ [6]

4. Implement the following Boolean function by a Hazard free OR-AND network.
   $f = \sum m(1, 3, 4, 5)$ and explain in detail what are the Hazards encountered in implementing the above function. [16]

5. Write a brief note on:
   (a) Architecture of PLDs
   (b) Capabilation and the limitations of threshold gates. [8+8]

6. (a) Explain the following
      i. Race-around condition in flip flop
      ii. J-K Master slave flip flop
      iii. Excitation table for flip flops. [3×2=6]
   (b) Draw the state diagram of modulo-4 up/ down counter. Design its circuit using J-K flip flops. [10]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   (a) Obtain State - Diagram.
   (b) Also obtain state - Table.
   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.
   (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

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