Code No: R5210504 **R5**

II B.Tech I Semester(R05) Supplementary Examinations, May/June 2010
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) List the first 20 numbers in base17. Use the letters A, B, C, D, E, F and G to represent the last seven digits. [4]
   (b) Convert the following numbers with the given radix to decimal.
   i. 1234_5
   ii. 1234_7
   iii. 1234_{11}
   iv. 333_4 [3+3+3+3]

2. (a) Write short notes about the various digital logic families.
   (b) Obtain the complement of the following Boolean expressions.
   i. AB + A(B + C) + B'(B + D)
   ii. A + B + A'B'C.
   (c) Obtain the dual of the following Boolean expressions. [8+4+4]
   i. A'B + A'BC' + A'BCD + A'BC'D'E
   ii. ABEF + ABE'F' + A'B'EF.

3. (a) If $F_1(A,B,C,D) = \sum(1,3,4,5,9,10,11) + d6,8$ And $F_2(A,B,C,D) = \sum(0,2,4,7,8,15) + d9,12$ Obtain minimal SOP expression for $F_1 \oplus F_2$ using K- map and draw the circuit using NAND gates.
   (b) Draw the multiple -level NAND circuit for the following Boolean - expression: $\left(A\overline{B} + C\overline{D}\right)E + BC\,(A+B)$ [8+8]

4. (a) Implement full adder with two 4 to 1 multiplexers. (Use block diagram for multiplexer)
   (b) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 × 1 multiplexer. (Use only block diagram). [8+8]

5. (a) Explain the operation of R-S master slave flip-flop. Explain its truth table.
   (b) Explain the operation of master slave J-K flip-flop with neat sketch. Distinguish with edge triggering. [16]

6. (a) Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.
   (b) Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram. [8+8]

7. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.
   (b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.
   ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
   iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. [8+8]

8. (a) Describe the analysis procedure of asynchronous sequential logic using flow table
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]
   $Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$
   $Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$
   $z = x_2 + y_1$
   i. Draw the logic diagram of the circuit.
   ii. Derive the transition table and output map.
   iii. Obtain a flow table for the circuit.

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