II B.Tech I Semester(R07) Supplementary Examinations, May/June 2010 SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical \& Electronic Engineering, Electronics \& Instrumentation Engineering, Electronics \& Control Engineering and Electronics \& Computer Engineering) Time: 3 hours

Max Marks: 80

## Answer any FIVE Questions <br> All Questions carry equal marks *****

1. (a) What is the necessity of binary codes in computers?
(b) Encode the decimal numbers 0 to 9 by means of the following weighted binary codes.

| i. 8 | 4 | 2 | 1 |
| :--- | :--- | :--- | :--- |
| ii. 2 | 4 | 2 | 1 |
| iii. 6 | 4 | 2 | -3 |

(c) Determine which of the above codes are self complementing and why?
2. (a) Find the complement of the following Boolean functions:
i. $\mathrm{F}=\mathrm{AB}^{\prime}+\mathrm{A}^{\prime} \mathrm{B}$
ii. $F=\left(V^{\prime} W+X\right) Y+Z^{\prime}$
(b) Prove that OR-AND network is equivalent to NOR-NOR network.
(c) Implement the Boolean function $\mathrm{F}=\mathrm{A}(\mathrm{B}+\mathrm{CD})+\mathrm{BC}$ ' usingonly NOR gates. $[6+4+6]$
3. Simplify the following Boolean expressions using K-map and implement them using NOR gates:
(a) $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\mathrm{AB}^{\prime} \mathrm{C}^{\prime}+\mathrm{AC}+\mathrm{A}^{\prime} \mathrm{CD}^{\prime}$
(b) $\mathrm{F}(\mathrm{W}, \mathrm{X}, \mathrm{Y}, \mathrm{Z})=\mathrm{W}^{\prime} \mathrm{X}^{\prime} \mathrm{Y}^{\prime} \mathrm{Z}^{\prime}+\mathrm{WXY} \mathrm{Y}^{\prime} \mathrm{Z}^{\prime}+\mathrm{W}^{\prime} \mathrm{X}^{\prime} \mathrm{YZ}+\mathrm{WXYZ}$.
4. (a) Implement Full Adder using decoder and OR gates.
(b) Realize the Boolean function $\mathrm{T}(\mathrm{X}, \mathrm{Y} Z)^{\prime}=\Sigma(1,3,4,5)$ using logic gates for hazard free. $\quad[8+8]$
5. (a) Derive a PLA programming tabte for the combinational circuit that squares a 3 bit number.
(b) For a given 3-input, 4-output truth table of a combinations ckt, tabulate the PAL programming table for the ckt.

| Inputs |  |  | Output |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| x | y | z | A | B | C | $\overline{\mathrm{B}}$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 |  | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |

6. (a) Explain various PLD's with their specifications.
(b) Giving excitation table, Explain the operation of JK flip flop.
7. (a) Draw the diagram of mealy type FSM for a serial adder.
(b) Derive the state diagram for an FSM that has an input w and an output z. The machine has to generate $\mathrm{z}=1$, when the previous four values of w were 1001 or 1111 otherwise $\mathrm{z}=0$. Overlapping input patterns are allowed.
An example of the desired behaviour is
$\mathrm{w}=010111100110011111$
$z=000000100100010011$
8. (a) Explain the symbols used in an ASM chart with neat diagrams.
(b) What are the salient features of the ASM chart?
