Code No: RR210204 **RR**

II B.Tech I Semester(RR) Supplementary Examinations, May/June 2010
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) A person on SATURN possessing 18 fingers has a property worth (1,00,000)18. He has 3 daughters and two sons. He wants to distribute half the money equally to his sons and the remaining half to his daughters equally. How much his each son and each daughter will get in Indian currency?
   (b) An Indian started on an expedition to SATURN with Rs.1,00,000. The expenditure on SATURN will be in the ratio of 1:2:7 for food, clothing and traveling. How much he will be spending on each item in the currency of SATURN.

   [8+8]

2. (a) Simplify the function using Karnaugh map method
   F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).
   (b) Give three possible ways to express the function
   F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals. [8+8]

3. Use tabular procedure to simplify the given expression
   f(v,w,x,y,z) =$\sum$m(0,4,12,16,19,24,27,28,29,31) in SOP form and draw the circuit using only NAND gates. [16]

4. (a) Give the implementation of a 4-bit ripple-carry adder using half- adder(s) / full-adder(s).
   (b) Explain with an example , the mux and demux can be used as data - selector and data-distributor respectively.

   [8+8]

5. (a) Draw the circuit diagram of J-K flip flop with NAND gates with positive edge triggering and explain its operation with the help of truth table. How race around condition is eliminated.
   (b) Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain.

   [8+8]

6. Design a modulo 6 up/down synchronous counter using T flip flops and draw the circuit diagram. [16]

7. What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

   [16]

8. (a) Draw the state diagram and the state table of the control unit for conditions given below. Draw the equivalent ASM chart leaving the state box empty.
      i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
      ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
      iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
      iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.
   (b) Design the control unit with multiplexers for the above problem

   [8+8]

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