Code No: RR310201



III B.Tech I Semester(RR) Supplementary Examinations, May 2011 COMPUTER ORGANIZATION

(Common to Electrical & Electronics Engineering, Electronics & Instrumentation Engineering, Electronics & Communications Engineering and Instrumentation & Control Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. (a) Define PCI. Explain the applications of PCI
 - (b) Describe any ten mandatory PCI signals.

[8+8]

- 2. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
 - i. 111.01 + 10.111
 - ii. 110.11 111.01
 - (b) Explain steps involved in the addition of numbers using 2's complement notation.

[10+6]

- 3. (a) Discuss various aspects of instruction set design.
 - (b) Explain about various types of data on which machine instructions operate.

[10+6]

- 4. (a) List and describe all arithmetic instructions of MIPS R-Series processors
 - (b) Discuss how R3000 pipeline can be modified to improve performance

[8+8]

- 5. (a) What is block hit ratio?
 - (b) Explain major variables on which hit ratio depends.
 - (c) Discuss about FIFO replacement with two different memory capacities. Give suitable example [3+3+10]
- 6. (a) What is multiple-platter disk.
 - (b) Differentiate between fixed and movable head disks.
 - (c) Define 'disk access time', 'seek time' and 'rotational latency'.

[5+5+6]

- 7. (a) Differentiate between micro programmed and hard wired control units with merits and demerits of each.
 - (b) Discuss about the design considerations of micro instruction sequencing technique. [8+8]
- 8. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
 - (b) How would you determine the number of pipeline stages in a pipelined processor [10+6]
