Code: R7411001

R7

IV B.Tech I Semester (R07) Supplementary Examinations, May 2012
VLSI DESIGN
(Common to Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE questions
All questions carry equal marks
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1. (a) Draw and explain the n-well process.
   (b) Explain the twin tub process with a neat diagram.

2. (a) Explain the CMOS inverter DC characteristics.
   (b) Discuss the small signal model of an MOS transistor.

3. (a) Explain in detail about stick diagrams.
   (b) Explain about lambda-based design rules.

4. (a) Explain in detail about propagation delays.
   (b) Draw the characteristics of FAN-IN-and FAN-OUT.

5. (a) Design a logic gate network for the full adder:
   (i) Using two-level logic.
   (ii) Using multi-level logic.
   (b) Design a stick diagram for a serial adder cell.

6. (a) Explain in detail about CPLD's with relevant diagrams.
   (b) Explain briefly about PLA's

7. (a) What is the need of HDL synthesis in VLSI technology?
   (b) Explain about design verification tools.

8. Explain the chip level test techniques.

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