Code: R7421901

R7

B.Tech IV Year II Semester (R07) Advanced Supplementary Examinations June 2012

ADVANCED COMPUTER ARCHITECTURE

(Electronics and Computer Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain about measuring and reporting performance.
(b) Discuss about the levels of programs in decreasing order of accuracy of predition.

2 (a) Explain about the operations in instruction set.
(b) Explain operations for media and signal processing.

3 (a) What is data hazard? Explain the differentiate types of data hazards.
(b) What is instruction level parallelism?

4 (a) Explain about static branch prediction.
(b) Explain the users of VLIW approach.

5 (a) Explain about miss penalty and out - of - order execution process.
(b) What is the technique used to reduce cache miss penalty?

6 (a) What are the challenges of parallel processing?
(b) Explain about cache coherence.

7 (a) Explain about transaction flow benchmark.
(b) Explain the design of an I/O system.

8 (a) Explain about generic interconnection N/W.
(b) Explain about interconnection N/W media.

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