Code: R7 420404

R7

B.Tech IV Year II Semester (R07) Advanced Supplementary Examinations, June 2012

DIGITAL DESIGN THROUGH VERILOG

(Common to ECE and ECC)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 Write short notes on:
   (a) Programming language interface.
   (b) Concurrency.

2 (a) Write a verilog code for master slave JK flip flop using NAND gates.
   (b) Design module to illustrate use of the wand-type net and test bench with stimulation results.

3 (a) Explain forever loop.
   (b) Explain briefly about stratified event queue.

4 (a) Design CMOS switch with a single control line.
   (b) Write short notes on Bi-directional gates.

5 (a) Explain clearly about hierarchical access.
   (b) Design verilog module for right shifter.

6 (a) Draw an SM chart for the control unit.
   (b) Explain briefly about SM block with feedback.

7 (a) Write differences between FPGA and CPLD.
   (b) Explain clearly about dice roll controllers.

8 Give detailed cycle by cycle operation for 6805 instructions.

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