Code: 9A04306

R09

II B.Tech I Semester (R09) Supplementary May 2012 Examinations
DIGITAL LOGIC DESIGN
(Computer Science & Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Convert the following to binary & then to gray code
   (i) $AB33_{16}$ (ii) 1764_8.
   (b) Write a short note on weighted and non-weighted codes.
   (c) Subtract the following numbers using the 2's complement method.
   (i) +39-(+16) (ii) -33-(-57)

2. (a) Simplify the following expressions
   (i) $AB + \overline{AC} + A\overline{B}C(AB + C)$
   (ii) $\overline{A\overline{B} + ABC} + A(B + A\overline{B})$
   (b) Express the function $Y = A + \overline{B}\,C$ in
   (i) Canonical sop and
   (ii) Canonical pos form.
   (c) What is meant by duality in Boolean algebra.

3. (a) Draw the logic circuit for the following function using NOR gates, $Y = A + (B + \overline{C})(\overline{D}E + F)$.
   (b) Obtain minimal sum of products expression for the following function and implement the same using universal gates
   $$f(A, B, C, D) = \Sigma(0,2,3,5,7,8,13) + \Sigma_d\,(1,6,12)$$

4. (a) Explain carry propagation in parallel adder with a neat diagram.
   (b) Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer. (use only block diagram)

5. (a) Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain.
   (b) Find the equivalence partition and a corresponding reduced machine in standard form for the machine given below.

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

6. (a) Design a 4-b ring counter using T-flip flops and draw the circuit diagram and timing diagrams.
   (b) Write a HDL behavioral description of shift register.

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7. (a) Explain briefly different types of R_0M_s.
   (b) Implement the following Boolean functions using PLA

$$A(x, y, z) = \Sigma(1,2,4,6),$$
$$B(x, y, z) = \Sigma(0,1,6,7)$$
$$C(x, y, z) = \Sigma(2,6)$$
$$D(x, y, z) = \Sigma(1,2,3,5,7)$$

8. (a) Design an asynchronous circuit that has two inputs x_1 and x_2 and one output z. The circuit is required to give an output whenever the input sequence (0,0) (0,1) and (1,1) received but only in that order.
   (b) Define Races in asynchronous sequential circuits.

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