Code: R7210504 **R07**

II B.Tech I Semester (R07) Supplementary May 2012 Examinations
DIGITAL LOGIC DESIGN

(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max. Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Represent decimal number 8620 in (i) BCD and (ii) Excess -3 code.
   (b) Perform the arithmetic operations (+42)+(-13) and (-42)-(-13) in binary using the signed-2's-complement representation for negative numbers.
   (c) Determine the value of base x if $(211)_x = (152)_8$.

2. (a) Simplify the following Boolean expressions to a minimum number of literals.
   (i) $x'y + xy' + xy + x'y'$ (ii) $A'B(D' + C'D) + B(A + A'CD)$
   (b) Convert the following to the other canonical form:
   (i) $F(x, y, z) = \Sigma(1,3,7)$ (ii) $F(A, B, C, D) = \Pi(0,1,2,3,4,6,12)$

3. (a) Implement the function F with the following two-level forms: NAND-AND and NOR-OR
   $F(A, B, C, D) = \Sigma(0,1,2,3,4,8,9,12)$
   (b) Simplify the following Boolean functions by first finding the essential prime implicates:
   $F(A, B, C, D) = \Sigma(1,3,4,5,10,11,12,13,14,15)$

4. (a) A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority function.
   (b) A combinational circuit is defined by the following three Boolean functions. Design the circuit with a decoder and external gates.
   $$F_1 = X'Y'Z' + XZ$$
   $$F_2 = XY'Z' + X'Y$$
   $$F_3 = X'Y'Z + XY.$$

5. (a) Explain the working of a master-slave JK flip flop. State its advantages.
   (b) List the procedure to design a clocked sequential circuit.

6. (a) Design a shift register with parallel load that operates according to the following functions table.

Shift	Load	Register Operation
0	0	No change
0	1	Load parallel data
1	X	Shift right

   (b) Design a 4-bit synchronous counter with D flip flops.

7. (a) Draw a PLA circuit to implement the logic functions A'BC+AB'C+AC' and A'B'C'+BC.
   (b) Using ROM, design a combinational circuit which accepts 3 bit number and generates an output binary number equivalent to the square of input number.

8. (a) Explain the difference between
   (i) Synchronous and Asynchronous sequential circuits .
   (ii) Stable and unstable states.
   (b) Draw the logic diagram of product of sums expressions:
   $$Y = (x_1 + x_2')(x_2 + x_3)$$
   Show that there is a static- 0 Hazard when x_1 and x_3 are equal to zero x_2 goes from 0 to 1. Find a way to remove the hazard by adding one more OR gate.

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