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R7

B.Tech II Year I Semester (R07) Supplementary Examinations, May 2012

PULSE AND DIGITAL CIRCUITS

(Common to EEE and EIE)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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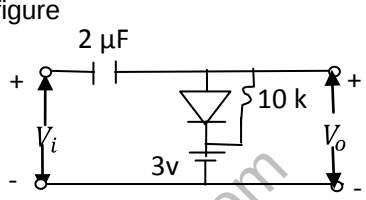
1 (a) Explain the operation of RC low pass circuit for exponential input is applied.
(b) Draw and explain the response of RLC circuits for step input.

2 (a) Explain the operation of positive clamper circuit using diode.
(b) Square wave whose pear to peak excursion are + 10V with respect to ground is impressed upon the diode clamping circuit shown in figure



The diodes has R_f = 100Ω, R_r = ∝ and V_r=0 sketch the steady state output waveform indicating clearly the voltage levels.

3 (a) Sketch neatly the waveforms of current and voltages for a transistor switch capacitance loading circuit.
(b) Explain the storage and transition times of the diode as a switch.

4 (a) What is a mono stable multi vibrator? Explain with the help of a neat circuit diagram the principle of operation of a mono stable multi vibrator.
(b) Explain how an Schmitt trigger circuit acts as a comparator.

5 Explain the basic principal of Miller and Bootstrap time base generators and also derive the equations for sweep speed error.

6 (a) Describe synchronization with: frequency division with neat waveforms.
(b) Explain the factors which influence the stability of a relaxation divider with the help of a neat wave forms.

7 (a) Write the applications of sampling gates.
(b) Distinguish between sampling gates and logic gates.

8 (a) Draw the circuit diagram of diode resistor logic. AND gate and explain its operation.
(b) Draw a pulse train representing a 11101011 in a synchronous positive logic digital system.
(c) Define a positive and negative logic systems.

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