

II B.Tech I Semester (R07) Supplementary May 2012 Examinations**SWITCHING THEORY & LOGIC DESIGN**

(Common to Electrical & Electronics Engineering, Electronics & Instrumentation Engineering,
Electronics & Control Engineering and Electronics & Computer Engineering)

Time: 3 hours**Max. Marks: 80**

Answer any FIVE questions
All questions carry equal marks

1. (a) Perform the following conversions:
 - (i) $(1938.257)_{10}$ decimal to hexadecimal.
 - (ii) $(713)_8$ Octal to binary.(b) What is the gray code? What are the rules to construct gray code?
(c) Encode data bits 1001 into a seven bit even parity Hamming code.
2. (a) Simplify the following Boolean functions to minimum number of literals:
 - (i) $F = ABC + ABC' + A'B$
 - (ii) $F = (A + B)'(A' + B')$.(b) Realize XOR gate using minimum number of NAND gates.
3. Simplify the following function using K- map and tabular methods. Compare the methods. Implement the result using NAND gates.
$$F(A, B, C, D) = \sum m(4, 5, 6, 7, 8) + \sum d(11, 12, 13, 14, 15).$$
4. (a) Explain how a 4 to 16 line decoder can be built using 2 to 4 line decoder.
(b) Design a four bit gray to binary code converter.
5. (a) A combinational circuit is defined by the functions
$$F_1(A, B, C) = \sum m(3, 5, 6, 7)$$
$$F_2(A, B, C) = \sum m(0, 2, 4, 7).$$
Implement the circuit using PLA.
(b) Discuss the concept of working and applications of the following memories: ROM, PAL and PLA.
6. (a) Define the following terms in connection to a flip flop.
 - (i) Set-up time.
 - (ii) Hold time.
 - (iii) Propagation delay.(b) Design a counter which goes through states in sequence 0, 2, 5, 7, 1.
7. (a) Write the differences between Mealy and Moore type machines.
(b) What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form

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7. (b)

PS	NS,Z X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

8. (a) Explain in detail the block diagram of ASM chart.
 (b) Draw the state diagram and the state table of the control unit conditions given below. Draw the equivalent ASM chart leaving the state box empty.
- (i) From 00 state, if $x=1$, it goes to 01 state and if $x=0$, it remains in the same state 00.
 - (ii) From 01 state, if $y=1$, it goes to 11 state and if $y=0$, it goes to 10 state.
 - (iii) From 10 state, if $x=1$ and $y=0$, it remains in the same state 10 and if $x=1$ and $y=1$, it goes to 11 state and if $x=0$, it goes to 00 state.
 - (iv) From 11 state, if $x=1$ $y=0$, it goes to 10 state and if $x=1$, and $y=1$, it remains in the same state, and if $x=0$, it goes to 00 state.
