Code: 9A04504

R09

III B. Tech I Semester (R09) Supplementary Examinations, May 2012

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) Design a three input NAND gate using diode logic and a transistor inverter. Analyze the circuit with the help of transfer characteristics.
(b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with VCC from 4.5 V to 5.5 V.

2 (a) Draw the circuit diagram of basic CMS gate and explain the operation.
(b) Discuss the steps in VHDL design flow.

3 (a) What is the importance of time dimension in VHDL and explain its function?
(b) Write a VHDL program to generate a clock with off time and on time equal to 10 ns.

4 (a) Using two 74×138 decoders design a 4 to 16 decoder.
(b) Write a data flow style VHDL program for the above design.

5 Explain about combinational multiplier with a neat diagram.

6 Write a structural VHDL program for counting number of ones in a 32 bit number.

7 (a) Design a self correcting 4 bit, 4 state ring counter.
(b) Design a self correcting 4 bit, 8 state ripple counter.

8 Design a 8X4 diode ROM using 74X138 for the following data starting from the first location 1, 4, 9, B, O, F, C.

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