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R9

B.Tech III Year I Semester (R09) Supplementary Examinations, May 2012

DIGITAL SYSTEM DESIGN

(Computer Science and Systems Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

Draw neat diagrams wherever necessary

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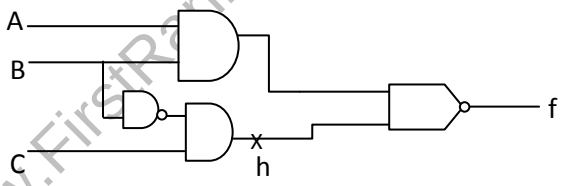
1 (a) What are the basic elements of an ASM chart? Explain with an example.
(b) Discuss briefly control sequence method.

2 (a) Describe important features of FPGA and CPLD.
(b) With an example how an CPLD is useful in the design of a digital circuit.

3 (a) Discuss the different faults found in combinational circuit.
(b) Explain Kohavi algorithm with an example.

4 (a) With an example, explain the transition count testing method.
(b) Apply D-algorithm to detect 'h' SAO fault in the circuit given below and derive the test vectors.



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5 (a) Explain how Kohavi algorithm is useful in detection of fault in digital circuit.
(b) With an example explain state identification.

6 (a) List out and explain briefly how faults that may occur in PLAs.
(b) Write short notes on PLA folding.

7 (a) Explain the steps involved in PLA folding algorithm compact.
(b) With an example explain how test generation can be achieved in testing a PLA.

8 Explain with examples:
(a) Fundamental mode model.
(b) Cycle and hazards.

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