Code: 9A04502

R09

III B. Tech I Semester (R09) Supplementary Examinations, May 2012

**LINEAR IC APPLICATIONS**

(Electronics & Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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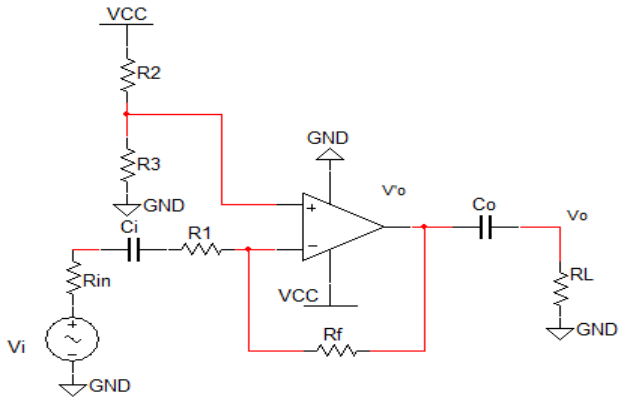
1 (a) Draw the equivalent circuits of emitter coupled differential amplifier from which calculate $A_d$.
(b) Draw the block diagram of four stage cascaded amplifier. Explain the function of each block.

2 (a) Discuss the electrical characteristics of an OP-AMP in detail.
(b) Discuss the three basic types of linear IC packages and briefly explain the characteristics of each.

3 For the inverting amplifier with a single supply shown below determine:
(a) Band width. (b) Maximum ideal voltage swing.
(c) Sketch output waveforms $V_O$ and $V_O$ if $V_{in}$ = 200 mV peak sine wave at 1 KHz.
If $R_1$ = 10 KΩ, $R_2 = R_3 = R_f$ = 100 KΩ, $C_i = C_O$ = 0.1 μF.




4 (a) Design a saw tooth wave form generator using OP-AMP and plot the waveforms for the given specifications: frequency: 5 KHz, $V_{sat}$= ± 15 V. (Assume necessary data).
(b) Explain how an operational amplifier is used as a basic comparator.

5 (a) Find the order of a low pass filter which provider -60 dB attenuation at $w/w_0$ = 2.
(b) Design a third order Butterworth low pass with upper cutoff frequency 1 KHz.

6 (a) Configure a 555 timer as a Schmitt trigger and explain.
(b) Explain frequency translation and FSK demodulation using 565 PLL.

7 (a) Classify commonly available analog to digital converters.
(b) Describe the operation of successive approximation type analog to digital converter.

8 Derive the output voltage expression for:
(i) Analog voltage multiplier circuit. (ii) Analog voltage divider circuit.
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