Code: 9A10504

R9

B.Tech III Year I Semester (R09) Supplementary Examinations, May 2012

LINEAR AND DIGITAL IC APPLICATIONS

(Common to E.Con.E, EIE and ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Derive the expression for CMRR for an emitter coupled differential amplifier.
(b) Define the DC and AC characteristics of OPAMP.

2 (a) Draw the circuit of a Full wave precision rectifier and explain the operation with necessary analysis.
(b) Draw and explain the operation of triangular wave generator using OPAMP.

3 (a) Draw the internal diagram of IC 555 timer and explain its operation as Astable multivibrator.
(b) Design an PLL circuit using IC 565 for a free running frequency of 400 kHz and capture range of ± 10kHz with a supply voltage of ± 6 V.

4 (a) Explain the CMOS dynamic electrical behavior.
(b) With a neat circuit diagram explain the operation of CMOS NOR Gate.

5 (a) Explain in detail about:
(i) Open collector TTL. (ii) Tri-state logic in TTL.
(b) Explain in detail about comparisons of logic families.

6 (a) Explain in detail about:
(i) Functions and procedures. (ii) Libraries and packages in VHDL.
(b) Discuss in detail about structural design elements in VHDL.

7 (a) Write the VHDL model for:
(i) Decoders. (ii) Encoders.
(b) Write the VHDL model for:
(i) Adders. (ii) Subtractors.

8 (a) Write the VHDL model for any one type of shift register.
(b) Explain in detail about synchronous design methodology.

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