Code: 9A04704

R09

B.Tech IV Year II Semester (R09) Advanced Supplementary Examinations, July 2013

DSP PROCESSORS AND ARCHITECTURES

(Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain in detail about the computational building blocks of DSP processors.
(b) Explain in detail the pipeline programming models.

2 Explain in detail the following sources of error in DSP implementation.
(a) A/D conversion errors.
(b) DSP computational errors.

3 Give a summary of the instruction set of TMS320C54XX processor with example.

4 Explain with butterfly computation, the overflow and scaling in FFT algorithms.

5 Explain with example the flash memory interface for the TMS320C54XX DSP.

6 (a) Explain VLIW architecture.
(b) Explain special addressing modes in programmable DSP's.

7 Write a program for the second order IIR filter.

8 Explain the comparison of the performances of the systems designed using FPGA's and digital signal processors.

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