R09

Code: 9A04706

B.Tech IV Year I Semester (R09) Supplementary Examinations, May 2013

DIGITAL DESIGN THROUGH VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks

****

1. (a) Write short note on the following:
   (i) Concurrency
   (ii) Simulation and synthesis
   (iii) Test benches.
   (b) Explain about the different data types in verilog HDL.

2. (a) Realize the edge triggered D flip-flop using NOR gate primitives.
   (b) Identify the ALU functions in the 8085 processors. Design an ALU module to carry out these.

3. (a) Design a 8-bit shift register module along with a test bench.
   (b) Explain about for loop in verilog with an example.

4. (a) Explain the operators used in dataflow level.
   (b) Design and simulate the ring counter in data flow level.

5. (a) Explain about system tasks and functions with one example.
   (b) Explain about the hierarchical access and also explain user defined primitives (UDP).

6. (a) Explain how you would realize SM charts using micro programming.
   (b) Explain clearly about linked state machine.

7. (a) Explain clearly about FLEX I0K series CPLDS.
   (b) Explaining about on hot state assignment.

8. (a) Write a note on design of micro controller CPU.
   (b) How would you interface a memory to a microprocessors bus?

******