Code: R7310404

R7

B.Tech III Year I Semester (R07) Supplementary Examinations, May 2013

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the circuit.

(b) Draw the CMOS circuit diagram of tri-state buffer. Explain the circuit with the help of logic diagram and function table.

2 (a) Draw the circuit diagram of basic CMS gate and explain the operation.

(b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00.

3 (a) Design the logic circuit and write a data-flow style VHDL program for the following function:

$$F(X) = \sum_{A,B,C,D} (0, 1, 3, 5, 14) + d(8,15).$$

(b) What is the importance of time dimension in VHDL and explain its function?

4 (a) Design a logic circuit to detect prime number of a 5-bit input.

(b) Using two 74 × 138 decoders design a 4 to 16 decoder.

5 Draw the logic symbol of 74 x 85, 4-bit comparator and write a VHDL code for it.

6 Write a VHDL code for 8 bit comparator circuit. Using this entity write VHDL code for 32 bit comparator. Show the additional logic used for this purpose and use structural style of modeling.

7 (a) Distinguish between the ring counter and ripple counters.

(b) Design a mod-129 counter using only two 74 × 163s and no additional gates.

8 Draw the structure and explain the operation of a ROM using MOS transistors as structural elements.

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