Code: 9A12301

R09

B. Tech II Year I Semester (R09) Supplementary Examinations, May 2013
DIGITAL LOGIC DESIGN & COMPUTER ORGANIZATION
(Common to CSS and IT)

Time: 3 hours   Max. Marks: 70
Answer any FIVE questions
All questions carry equal marks
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1   Draw the flowchart for multiplication of two fixed point numbers when negative numbers are in signed-magnitude representation and explain with an example.

2   Design a modulo-12 up synchronous counter using T-flip flops and draw the circuit diagram.

3   Explain about the two ways to achieve a BCD counter using a counter with parallel load.

4 (a) Explain how booths algorithm is suitable for signed number multiplication in comparison of conventional shift and add method.
   (b) Discuss the Booth's multiplication algorithm with an example.

5 (a) Write short notes on the following with an example:
        (i) Three-address instructions.
        (ii) RISC instructions.
        (iii) Machine instructions.
   (b) Explain about machine instruction sequencing techniques.

6 (a) List down the various basic operations a CPU has to perform for the execution of various instructions.
   (b) Explain with the help of a neat sketch how the building blocks of the processor units are organized and how they are interconnected.

7 (a) What is meant by cache coherency? Why is cache coherency necessary? Explain different approaches for cache coherency.
   (b) What is meant by virtual memory? What is the need to implement virtual memory?

8 (a) What is I/O interface? Explain I/O interface with the help of a block diagram.
   (b) With the help of a neat sketch explain the I/O interface for I/O device and I/O interface for O/P device.

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