Code: 9A15502

R9

B.Tech III Year I Semester (R09) Supplementary Examinations, May 2013

DIGITAL SYSTEM DESIGN

(Computer Science & Systems Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 (a) With an example, explain the use of ASM charts in the design of digital circuits.
(b) Discuss in detail about the following:
(i) Reduction of state tables. (ii) State assignment procedure.

2 (a) Describe important features of FPGA.
(b) Draw the general structure of a CPLD and explain how a logic function can be realized on CPLD with simple example.

3 (a) What is a fault? Give the classification of faults that may occur in digital circuits.
(b) Explain how Kohavi algorithm is useful in deflection of faults in digital circuits.

4 (a) Describe the algorithmic steps involved in PODEM.
(b) With a neat circuit diagram, describe the working of a signature analyzer.

5 (a) Give the steps involved in design of fault detection.
(b) For the machine M_1, shown below, find the shortest homing sequence.

MACHINE M_1

PS	X = 0	N_S, Z X = 1
A	A, 1	E, 0
B	A, 0	C, 0
C	B, 0	D, 1
D	C, 1	C, 0
E	C, 0	D, 0

6 (a) Describe the advantages of PLA minimization and folding.
(b) Describe the types of cross point fault that occur in PLA's.

7 (a) With an example, explain how faults are detected in a PLA.
(b) Discuss briefly about testable PLA design.

8 Write short notes:
(i) Flow model.
(ii) Minimal closed covers.
(iii) Cycles and hazards.

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