Code: R7220401

R07

B.Tech II Year II Semester (R07) Supplementary Examinations, April/May 2013

PULSE AND DIGITAL CIRCUITS

(Common to ECE, E.Con.E and ECC)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Obtain the relation between rise time and bandwidth of the low pass circuits.
(b) Calculate the lowest square wave frequency that can be passed by an amplifier with lower cutoff frequency of 10 Hz. If the output tilt is not to exceed 2%.

2 (a) With the help of a neat circuit diagram, explain the working of a two level diode clipper.
(b) Explain principle of clamping. What is the need for shunting resistor R in parallel with diode in basic clamping circuit?

3 (a) Explain in detail about junction diode-switching timer.
(b) With a neat circuit diagram and necessary wave forms, explain the operation of a transistor switch.

4 (a) With the help of a neat circuit diagram and wave forms, explain the working of a Schmitt trigger.
(b) Derive an expression for frequency of oscillation of an astable multi-vibrator.

5 (a) Explain in detail about basic principles of Miller and Boot strap time base generators.
(b) With the help of a neat circuit diagram, explain the working of a simple current sweep.

6 (a) With the help of a circuit diagram and waveforms, explain the frequency division by an astable blocking oscillator.
(b) Explain the synchronization of sweep by a symmetrical signal.

7 (a) With the help of a neat diagram, explain the operation of a two diode sampling gate.
(b) With the help of a neat diagram, explain the working of a bidirectional gates using transistors.

8 (a) With the help of a neat circuit diagram and truth table, explain the working of a:
(i) DL OR gate
(ii) RTL OR gate

(b) With the help of a neat circuit diagram and truth table, explain the working of a:
(i) DTL NAND gate
(ii) RTL NAND gate

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