Code: 9A04605

R09

B.Tech IV Year II Semester (R09) Advanced Supplementary Examinations, July 2013

VLSI DESIGN

(Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 Explain clearly about p-well CMOS fabrication process with neat diagrams.

2 Mention different non ideal I-V effects and clearly explain about them.

3 What are the advantages of scaling? Distinguish between constant field scaling and lateral scaling.

4 What is the problem of driving large capacitance load? Explain a method to drive such load.

5 (a) Make a comparison between dynamic and static memory cells.

(b) With the help of a diagram explain the architecture and working of memory arrays?

6 Explain how does the delay and area grows with the number of data input in a multiplexer.

7 (a) By considering a sea of gate array (SOG), design the wiring that would construct a logic function.

$$f = \overline{ABC + AB\overline{C}}.$$

(b) Using VHDL as a tool synthesizes the structural design of a RAM.

8 (a) What is a level sensitive logic system?

(b) With suitable diagram explain the principle of testing through LSSD approach.

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