R07

Code: R7411001

B.Tech IV Year I Semester (R07) Supplementary Examinations December 2015

**VLSI DESIGN**

(Common to EIE and ECC)

(For 2008 regular admitted batch only)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) With neat sketches explain CMOS fabrication using p-well process.
(b) Compare CMOS and bipolar technologies.

2 (a) Determine the pull up and pull down ratio for an nMOS inverter driven by another nMOS inverter.
(b) Explain Latch up problem in CMOS circuits.

3 Design a stick diagram and layout for CMOS logic shown below:
$Y = \overline{(AB + CD)}$

4 (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
(b) Calculate the gate capacitance value of 5 nm technology, minimum size transistor with gate to channel capacitance value is $4 \times 10^{-4}$ pF/$\mu m^2$.

5 (a) Draw the schematic for tiny XOR gate and explain its operation.
(b) Design a magnitude comparator based on the data path operators.

6 (a) Draw and explain the architecture of FPGA.
(b) Explain how the I/O pad is programmed on FPGA.

7 With respect to synthesis process explain the following:
(a) Flattening.
(b) Factoring.
(c) Mapping.

8 (a) What type of faults can be reduced by improving layout design?
(b) Draw the state diagram of TAP controller and explain how it provides the control signals for test data and instruction register.

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