Code: 9A04704 **R09**

B.Tech IV Year I Semester (R09) Regular & Supplementary Examinations December 2015

DSP PROCESSORS & ARCHITECTURES

(Common to ECE & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) What are the advantages and disadvantages of programmable DSP processors?
(b) Explain about address generation unit in a DSP.

2 (a) Explain the sources of errors in DSP implementations.
(b) Explain about A/D conversion errors and D/A conversion errors.

3 (a) Discuss about DSP computational building blocks and explain all blocks clearly.
(b) Design an address generation unit for programmable DSP architecture.

4 (a) Explain the memory organization in TMS320C54XX DSP.
(b) Explain the pipeline operation of TMS320C54XX processor.

5 (a) Explain Q-notation with an example.
(b) Explain an adaptive filter with any simple program.

6 (a) Implement FFT algorithm for DFT computation.
(b) Write about 16-point FFT implementation on the TMS320C54XX.

7 (a) How memory interfacing is done in DSP's?
(b) Write a CODEC interface circuit.

8 (a) Describe design flow for an FPGA based system design.
(b) Discuss about algorithm for implementation of filters in VLSI.

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